

FIG. 1

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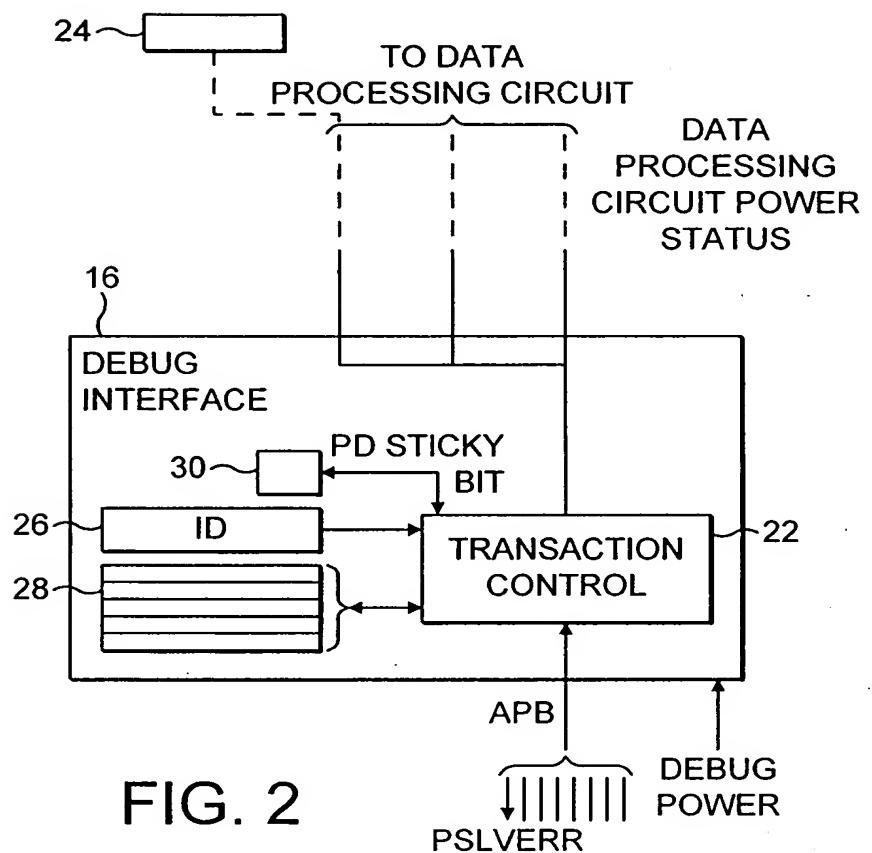


FIG. 2

POWER DOWN STICKY BIT SETTING

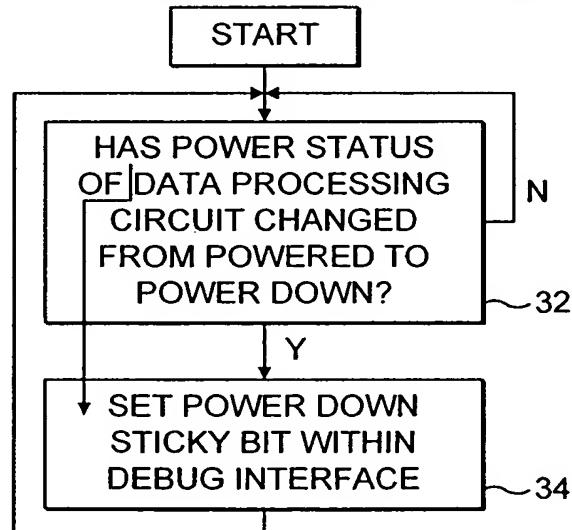


FIG. 3



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DEBUG BUS ERROR GENERATION

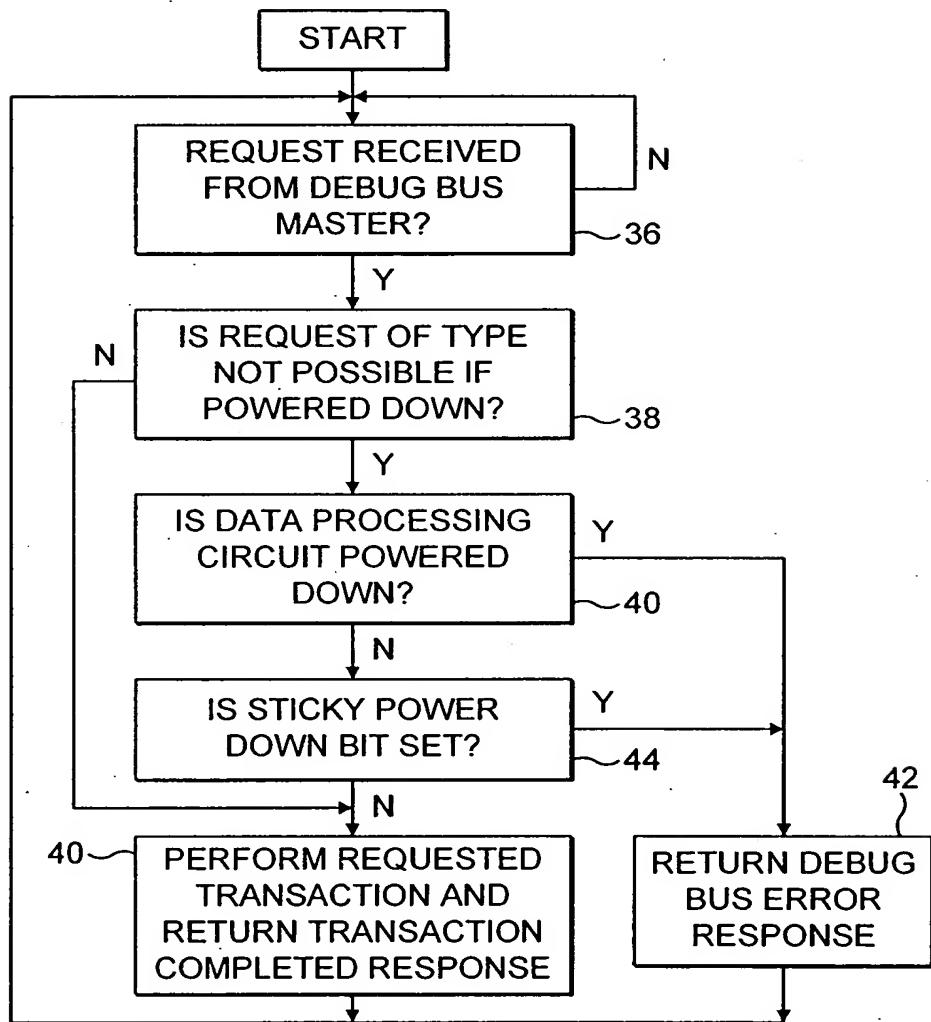


FIG. 4